



SSP and SPI Code

General Structure

SSP and SPI code is written such that there is a shared common set of functions with a unique structure passed into the general task code that differentiates devices. Each SSP or SPI interface in the system is managed by its own task.

Each device that can be attached to an SSP/SPI bus has a unique command and data set. These are handled by higher level tasks which are layered on the SSP/SPI tasks.

Data passed to the SSP/SPI task include a chip select structure which names application functions to assert and negate hardware chip select signals.

Linear Technology ADC

A task is provided which communicates with Linear Technology ADCs.

Ramtron FRAM Devices

A task is provided which communicates with Ramtron FRAM devices to read and write memory locations.

Serial Shift Register

A function to write a value to a shift register, (595 type) is included.

Slave Mode

Code is provided to be a slave SSP/SPI device. This enables two processors to communicate via SSP/SPI hardware where one is the master and the other the slave.